Daily Briefing: News Snippets

Military EMBEDDED SYSTEMS

VOLUME 7 NUMBER 8
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COLUMNS

DEPARTMENTS

ON THE COVER:
Joint Tactical Radio System (JTRS) is currently being demonstrated and evaluated by the Army with some variants scheduled for delivery in 2012. Photo courtesy of General Dynamics C4 Systems.

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AFCEA West
January 24-26, 2012 • San Diego, CA
http://www.afcea.org/events/west/12/introduction.asp

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Show me the weapon system, no more PowerPoints please

By John McHale, Editorial Director

If suppliers from the primes on down plan on making calls on Army, Air Force, Navy, or Marine program managers, they best leave their PowerPoint slides at home. U.S. DoD leaders say they are tired of sitting through presentations on how a product might work if it needs government funding to be developed.

Better than just a PowerPoint slide, the military needs products and systems that meet requirements and can be put into a demonstration quickly for testing, said Maj. Gen. William Crosby, Program Executive Officer, Army Aviation command during a press briefing at the annual meeting of the Association of the U.S. Army (AUSA) earlier this fall.

The Army and other branches are essentially asking industry to pick up part of the development tab.

"Our country has a budget challenge; we have to work closely with partners in industry and do the best we can with what we have" – accepting the risk and maintaining an active priority list, said Maj. Gen. Tony Crutchfield, Army Aviation branch chief, at the AUSA press briefing.

The Army is "determined to try it before they buy it," Mike Madsen, President of Defense & Space for Honeywell Aerospace in Phoenix told me at AUSA. "It is expected that there will be more cost sharing and we would echo [the Army's] concern that they get a good demonstration and see the product in action before they make a decision to purchase."

Developing systems and products for military applications without DoD funding is not a new phenomenon, but has been happening for some time and with success.

For example, Harris RF Communications developed the Falcon III AN/PRC-117G Software-Defined Radios outside of the Joint Tactical Radio System (JTRS), but compliant with the program requirements. However, because Harris developed them with their own money, they were able to field them way ahead of the JTRS program.

The DoD is going to be moving development costs back toward the suppliers, said Sean Jordan, Vice President of Finance for the FLIR Systems Government Systems division in Wilsonville, OR. During The FLIR AUSA press briefing, Jordan said that his company's electro-optics and other systems have mostly always been self-funded, so they feel they are also well positioned to take advantage of the new procurement trend.

Embedded COTS component suppliers have been funding their own designs for some time, offering the embedded boards, connectors, hard drives, and so on, that are ready to work right away with just minor tweaks.

COTS suppliers proved that rugged military quality equipment can be delivered off the shelf without excessive government funding required for development.

Now it seems that this process is moving right on up the food chain.

Another COTS procurement characteristic appearing at the program level is the embrace of open architectures and standards over old stovepipe, proprietary systems that are not compatible with new technology or other DoD platforms.

A popular phrase in DoD circles these days is "platform agnostic." In other words, having systems and technology that are not tied to one specific platform.

An example of this is the DoD's common ground control segment, being designed by industry and the DoD to create a common architecture to be used across all unmanned aerial system platforms. Essentially, the DoD wants to eliminate the costs of having proprietary ground control stations for Unmanned Aerial Vehicles (UAVs). Every UAV prime contractor has ground control stations that only work with their specific UAV.

Having a common ground control segment that is platform agnostic would save costs in the long run.

Platform agnosticism is also behind the cancellation of the JTRS Ground Mobile Radio (GMR) program. Instead of funding the GMR from the ground up, Pentagon planners will be turning to industry to come up with solutions from current technology to meet the GMR requirement. (For more on JTRS, see the special report on page 16.)

Having architectures and technology shared among different platforms will also improve warfighter training on the new systems – by reducing training time and costs.

Crutchfield said during the AUSA press conference that training is often overlooked when discussing funding for platforms and upgrades.

"In these trade shows, it is easy to concentrate on material solutions and the numbers associated with those solutions," but often the cost of training gets overlooked, Crutchfield said. "As the user, I have to make sure it's affordable because we have to train" them to use the new systems and that will not be inexpensive in any way.

"Sometimes in trade shows that gets missed, and I want to make sure that we all keep that in mind."

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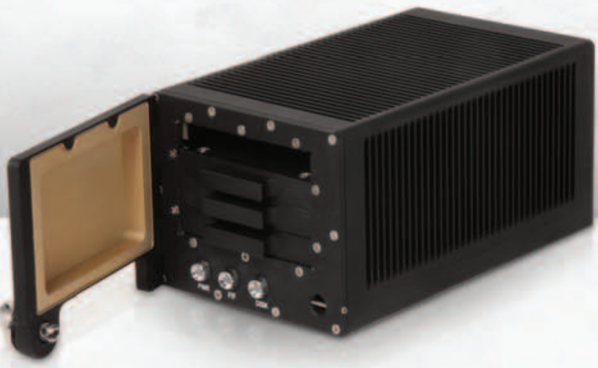

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Enhancing MIL-STD-1553's bit rate

By Duncan Young

Continued budget restrictions are causing many aging military aircraft and ground vehicles to be deployed with little prospect of replacement. However, these platforms must be sustained and upgraded, preferably with as little disruption to wiring harnesses as possible. Hence, standards like MIL-STD-1553B that were installed when these platforms were built continue to have long lifespans. New types of capabilities such as miniature smart bombs and rockets require all the beneficial characteristics of 1553 such as determinism, low latency, redundancy, and noise immunity, plus widespread developer familiarity, but at higher bit rates and lower cost per connection.

Avionics architecture

MIL-STD-1553B runs at 1 Mbps using a multidrop redundant bus architecture with a single Bus Controller (BC) and multiple Remote Terminals (RTs). A Bus Monitor (BM) might be included to record and time-tag all bus activity. 1553 uses a deterministic command/response protocol; the BC is typically programmed to operate at a 30 Hz frame rate to interrogate RTs and transfer data to or from attached subsystems. The frame rate and low bit rate determine the system architecture. For example, a typical system might have a mission computer attached via MIL-STD-1553B to many subsystems such as sensors, communications, electronic warfare, stores management, and so on. This is generally referred to as *federated architecture*, wherein each subsystem needs a great deal of processing and data reduction before transmission to the mission computer.

Federated architecture determines upgrade strategy. If only a few subsystems need to be upgraded or replaced, it is more cost-effective to keep the existing cabling, frame rates, and data transmission concept. It is equally difficult to upgrade a mission system to a faster version of 1553 unless all the subsystems are also revised simultaneously. In this case, it might be beneficial to move to other fabrics such as Fibre Channel and a more integrated avionics architecture.

Subsystem level

It might not be cost-effective to replace an entire 1553 backbone, but subsystem upgrades will introduce greater performance, capability, and complexity. External interfaces can be MIL-STD-1553B, for example, as part of a MIL-STD-1760 stores interface.

The introduction of new, highly capable smart munitions identified the need for a faster, cheaper interface than 1553B, prompting development of the 10 Mbps Miniature Munitions Stores Interface (MMSI), also known as SAE-AS5652 Enhanced Bit Rate (EBR) 1553. The greater performance of EBR-1553 allows rapid reprogramming of smart munitions and supports the development of more generic fire control/stores management computers that can handle a broader mix of smart weapons.

Topology

EBR-1553 is connected in a star topology radiating from the BC to each RT using RS-485 differential signaling for high levels of noise immunity. Cabling uses regular 1553 Twinax, with each star connection representing a unique RT address. Notwithstanding the revised topology, from a user's perspective, EBR-1553 retains the deterministic command/response characteristics of MIL-STD-1553B, enabling the development of frame patterns and data flows to suit the application in the same manner as 1553. The performance potential of 10 Mbps and its 1553-like operation make EBR-1553 suitable not only for stores management applications, but also for many other ground and airborne upgrade projects. More complex subsystems or clusters of subsystems that require faster frame rates or greater data transfer capability than the platform's 1553 bus are possible, plus gateways to new functions or capability can be created.

Embedding EBR-1553

MIL-STD-1553B is perhaps the most widely deployed standard for military and aerospace applications. With thousands of instances in the field, the interface has been embedded into systems and subsystems using discrete devices and IP cores in FPGAs, integrated onto SBCs, and added as mezzanine modules. Similar flexibility exists for implementation of EBR-1553 (Figure 1). Individual RT implementations as typically found in small, high-volume smart munitions can be very low cost, requiring only RS-485 transmit and receive components plus an FPGA or integrated processor device. A PMC offers an ideal form factor for more complex implementations within a CompactPCI, VMEbus, or VPX (VITA 46) embedded computing subsystem. The PMC-MMSI from GE Intelligent Platforms, for example, supports all EBR-1553 types and up to 12 terminal lines.

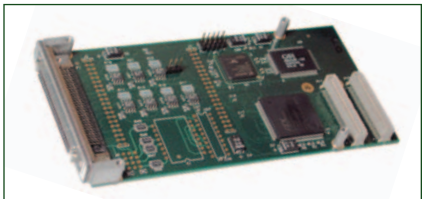

Figure 1 | PMC-MMSI EBR-1553 mezzanine module from GE Intelligent Platforms

MIL-STD-1553B will continue to be deployed for as long as the platforms that have it installed remain in active service, many of them with decades of useful life remaining. EBR-1553 offers additional performance and capability that can be easily integrated into new and upgraded subsystems without disturbing the platform's system architecture and cable infrastructure.

To learn more, e-mail Duncan at duncan_young1@sky.com.

Lead-free technology in mil/aero electronics

By Steve Edwards

The European Union's Restriction of the use of certain Hazardous Substances (RoHS) Waste Electrical and Electronic Equipment (WEEE) directives ban the use of lead and five other substances in many electronics applications. As the lead-free movement grows worldwide, the scarcity of lead-containing electronic components will increase. These components form the foundation of advanced technology Aerospace and Defense (A&D) applications.

Today, A&D applications, which are not explicitly named in RoHS and WEEE, can continue using components that contain lead. Even so, to ensure reliability in harsh environments, it is essential to understand the impact that lead-free COTS components might have on advanced technology military applications.

The "tin whiskers" phenomenon is a well-known issue related to the use of lead-free devices in A&D applications. But many other effects including pad cratering, PCB delamination, and solder joint cracking must be understood and addressed to ensure that the industry can continue producing reliable high-performance electronics.

The Pb-free Electronics Risk Management (PERM) Consortium, formerly known as Lead-Free Electronics in Aerospace Project (LEAP), has published several important standards addressing control and management of lead-free issues. An outgrowth of the PERM Consortium project, the Lead-Free Electronics Manhattan Project (LFEMP) group, has identified numerous technical risks associated with using lead-free electronics in A&D applications. So far, the LFEMP group has produced two reports titled *Phase I* and *Phase II*. *Phase I* identified best practices with lead-free and highlighted significant gaps that require investigation and resolution for A&D electronics. The *Phase II* draft report details these gaps and presents a comprehensive and coordinated three-year Pb-free Electronics Risk Reduction (PERR) project to address them. The next report, *Phase III*, is intended to execute the PERR project.

Lead-free reliability risk for A&D electronics

The Phase II draft report outlines five top-level R&D project areas to deal with technical risks and knowledge gaps for the use of lead-free electronics in A&D applications: tin whiskers, electronics assembly, solder joints, PCBs, and components. Once the PERR project is funded, its activities are expected to take three years, with the aim of resolving most lead-free technical issues for A&D electronics.

Meanwhile, three main approaches are available to COTS module suppliers for dealing with lead-free components:

1. Reball area array components to tin-lead and solder with tin-lead solder
2. Accept lead-free components and solder with lead-free solder (predominantly SAC305)
3. Take lead-free components and solder with tin-lead solder

Approaches for lead-free electronics

The first approach can elevate lead-free electronic assemblies close to the baseline solder joint reliability of tin-lead. Concerns about tin whiskers can be mitigated with techniques such as solder dipping of non-BGA components and/or conformal coating. Concerns about reliability due to additional heat exposure and handling needed for component reprocessing can be mitigated through appropriate process controls. This first approach incurs the highest direct costs.

The second approach, popular outside of A&D and other high- reliability industries, is favored by some in the COTS industry because of lower direct costs and reduced lead-time impact. However, it might not address the reliability risks and knowledge gaps detailed in the LFEMP reports. To aid the customer, vendors should demonstrate how these risks and knowledge gaps are addressed. A large amount of data such as thermal cycling is available for some aspects of this approach, but details regarding applicability to specific products need to be assessed. COTS vendors should be able to produce lead-free test data such as extended temperature cycling, vibration in A&D environments on COTS components and assemblies, and compare data to tin-lead and mixed-solder approaches.

In the third approach, area array components such as BGAs with lead-free solder balls are soldered with tin-lead solder. This combines lower costs and reduced lead-time impact (no component reprocessing) with less perceived risk (tin-lead solder). Some studies have indicated acceptable thermal cycling reliability using commercial temperature ranges, while other studies have shown inconsistent reliability across several component packages using an extended temperature range. Overall, the details of this approach including solder microstructure, strength, fatigue, and acceleration factors are less understood than the lead-free approach.

Curtiss-Wright Controls Embedded Computing (CWCEC) has extracted a list of reliability risk factors from the LFEMP reports. Following extensive testing and analysis including the impacts of risk mitigations, CWCEC can guide customers in evaluating the reliability of lead-free approaches. For more information on the use of lead-free devices in COTS applications, see www.cwcembedded.com/lead_free.htm.

To learn more, e-mail Steve at Steve.Edwards@curtisswright.com.

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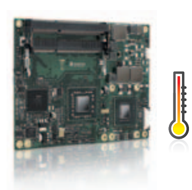

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Daily Briefing: News Snippets

By Sharon Hess, Managing Editor

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Command Web: Google + laptops = Army operational picture

Apparently the ubiquitous use of Google products and laptops hasn't gone unnoticed by the U.S. Army and Lockheed Martin. The evidence: the Lockheed Martin-incarnated Command Web Internet-based system is being tested in the field. Command Web enables warfighters in theater and commanders in C2 centers to see a common battlefield operational picture via Google Earth and a laptop (Figure 1). Command Web's purpose is to bring U.S. Army tactical network access to all operational users to render actionable mission data, while its Web foundation decreases logistical support footprints. Based on the NSA's Ozone framework, Command Web is interoperable with the Internet-based Distributed Common Ground System – Army (DCGS-A) ISR program. Additionally, Command Web features an interface design that mimics the naming conventions and functionality of Army Battle Command Systems, the Army's main viewer of the common operational picture, currently utilized in all theaters. Testing includes the user interface design, requirements, and system architecture.

Figure 1 | In-theater testing of the Lockheed Martin-developed Command Web rolls on. Command Web joins Google Earth and a laptop, to provide a common battlefield operational picture to warfighters and commanders. Stock photo

Northrop Grumman: 1 down, 9 to go

USMC deployment of the first AN/TSQ-269 Mobile Tactical Air Operations Module (MTAOM) C2 system has occurred, with 9 more to follow shortly. MTAOM is designed to enable the Tactical Air Operations Center's direction of air-defense and C2 operations everywhere, and is "a self-contained, expeditionary platform," the company reports. It comprises mobile components such as Multi-Radar Tracker (MRT) processors, the AYK-14 Replacement Computer (ARC) circuit card weighing 5 oz. and acting as the MTAOM's primary computing center, and tactical data link support units. Now in use by the Marine Air Control Squadron 1, the platform has digital communications and processor equipment housed inside the S-788 High Mobility Multipurpose Wheeled Vehicle shelter and renders support for as many as 20 control-operator and air-command workstations.

Trio of contracts to improve SM-3

Clearly, the Standard Missile-3 (SM-3) Block IIB is on the minds of officials at the Missile Defense Agency (MDA). Granted identical MDA contracts (except for the dollar amounts): Aerojet at $15 million and United Technologies Corp., dba Pratt & Whitney Rocketdyne, Inc., at just shy of $14 million. Both companies were commissioned to develop and test attitude-control and liquid-divert system technologies. The goal is to decrease risk and boost performance of the SM-3 Block IIB, and work under both contracts proceeds through September 2013. The third MDA-issued SM-3 Block IIB contract was awarded to Alliant Techsystems (ATK), Inc. at $9.5 million. The contract specifies that "ATK will develop and test specific third-stage rocket motor technologies of interest to the MDA." With part of its total value funded by fiscal 2011 RDT&E funds, the goal of the ATK contract is the same as the "twin" contracts' goals: to heighten performance while lessening risks of SM-3 Block IIB.

T-34 contract option could save lives

Keeping military aircraft such as the T-34 Turbomentor in top-top shape is imperative to saving lives, and a recent U.S. Navy/Sikorsky Support Services, Inc. contract modification aims to perpetuate that (Figure 2). Specifically, the $49 million option exercised on a formerly granted IDIQ contract stipulates that Sikorsky renders materials and services for depot-level, intermediate, and organizational maintenance for 62 T-6, 54 T-44, and 273 T-34 aircraft housed mainly at Naval Air Station (NAS) in Pensacola, FL; NAS Whiting Field, FL; and NAS Corpus Christi, TX. Contract completion is slated for next February, and the contracting activity is the Naval Air Systems Command in Patuxent River, MD.

Figure 2 | A recent $49 million contract modification stipulates that Sikorsky Support Services, Inc. renders materials and services for depot-level and other maintenance for U.S. Navy T-6, T-44, and T-34 (pictured) aircraft. U.S. Navy photo by Richard Stewart

Boeing gives support, to the tune of $11 billion

With the first C-17 taking its maiden voyage back in 1991 and the first C-17 delivery to the military in 1993, the aircraft has come a long way since then (literally). Now the C-17 Globemaster III aims to benefit from a whopping $11 billion (maximum) IDIQ contract between the USAF and The Boeing Co (Figure 3). The contract specifies that Boeing is to afford sustainment and support to a government Product Support Manager (PSM)/ Product Support Integrator (PSI) for the weapon system tucked inside the C-17. Support consists of depot-level aircraft modifications and maintenance, Long-Term Sustainment (LTS) planning, F117 propulsion system management, equipment and material management, quality assurance, sustaining engineering, and more. Foreign Military Sales comprises about 10 percent of the contract, and includes Canada, Australia, Qatar, United Arab Emirates, the United Kingdom, and NATO Strategic Airlift Capability.

Figure 3 | The C-17 Globemaster III aims to benefit from a whopping $11 billion (maximum) IDIQ USAF/The Boeing Co. contract for sustainment and support services. U.S. Air Force photo by Tech. Sgt. Charles Vaughn

Acquisition activity gets the GoAhead

Oracle – purveyor of integrated, open hardware and software systems – announced its plans to acquire **GoAhead Software**, a vendor of COTS high availability software and middleware for mission-critical systems. While the sum of the transaction (which is expected to close later this year) has not been announced, the impetus is reportedly that the GoAhead acquisition will "help us deliver a comprehensive, standards-based, carrier-grade platform that supports the delivery of new services in the call path of the network," said Nigel Ball, Vice President, Oracle Communications Industry Solutions, in a media statement. Oracle presently serves diverse industries including defense and aerospace, automotive, high technology, life sciences, insurance, utilities, financial services, communications, engineering and construction, and chemicals, among many others.

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Figure 4 | The U.S. Army's IBCTs will soon be ready for conflict, per a recent $134 million U.S. DoD order to BAE Systems for 70 lightweight M777 Howitzers. U.S. Army photo by Spc. Evan D. Marcy, 55th Signal Company

BAE Systems to provide M777 Howitzers

The U.S. Army's Infantry Brigade Combat Teams (IBCTs) will soon be ready for conflict, per a recent $134 million U.S. DoD order to BAE Systems for 70 lightweight M777 Howitzers (Figure 4). This recent order raises the U.K./U.S. program's total gun count to 1,071, and extends the production timeframe to October 2013. What sets the lightweight M777 apart from conventional towed 155 mm systems is its relatively miniscule weight of <4200 kg (about half the "load"). Consequently, the nimble M777 can be transported easily via medium-lift helicopters "to otherwise inaccessible areas," the company reports. Prime contract management and some assembly and manufacturing events transpire at Barrow-in-Furness, U.K., and testing and final integration will occur at the BAE Systems locale in Hattiesburg, MS.

General Dynamics to aid LPD 22 availability

The LPD 22/USS San Diego amphibious transport dock warship is set to benefit from a recent General Dynamics NASSCO/ U.S. Navy contract for $37 million (Figure 5). Under the contract, General Dynamics will provide engineering, design, planning, scheduling, labor, program management, and incidental material procurement "for the fitting-out availability" of LPD 22. If activated, the contract's options raise the total value to nearly $135 million. Contract completion is anticipated in December of 2014, and fulfillment takes place in San Diego, CA. The contracting activity is the Naval Sea Systems Command in Washington, D.C.

Figure 5 | The LPD 22/USS San Diego is set to benefit from a recent General Dynamics NASSCO/U.S. Navy contract for $37 million for engineering, design, program management, and incidental material procurement. U.S. Navy photo courtesy of Northrop Grumman

Photo courtesy of General Dynamics C4 Systems

JTRS update: Radio systems move closer to deployment, while GMR gets cut

By John McHale, Editorial Director

Variants of the Joint Tactical Radio System (JTRS) program are on the verge of full deployment in 2012, yet the budget woes of 2011 have knocked out the JTRS Ground Mobile Radio system. Meanwhile, government and industry are evolving the technology behind JTRS – Software-Defined Radio (SDR) – with commercial smartphone technology to improve situational awareness for the warfighter.

Nearly 15 years after the initial concepts of the program were laid out, elements of the Joint Tactical Radio System (JTRS) are nearing their first deployment in 2012.

The JTRS program, designed to enable soldiers with different radios to communicate with each other by defining radio functionality in software, was created in 1997 as a group of replacements for various radio programs. After different evolutions and program reorganizations, the JTRS program is now under a Joint Program Executive Officer (JPEO) in San Diego with a specific goal to design a "family of interoperable modular, Software-Defined Radios (SDRs) that operate as nodes in a network that provides secure wireless communication and networking services for mobile and fixed forces, consisting of U.S. Allies, joint, and coalition partners, and in time, disaster response personnel," according to the JPEO.

The main elements of the JTRS program are the Handheld, Manpack, and Small Form Fit (HMS); Airborne, Maritime, and Fixed Station (AMF); the Multifunctional Information Distribution System (MIDS); and the Ground Mobile Radio (GMR).

Unfortunately, because of the current fiscal climate in Washington, U.S. Department of Defense (DoD) officials were forced to re-evaluate the GMR variant and subsequently cancel it. Boeing was the prime contractor for the GMR with Rockwell Collins and BAE Systems on its team.

DoD officials notified members of Congress on a decision to cancel the GMR in October, according to a spokesman for the JTRS JPEO in San Diego. The cancellation enables the Army to pursue "lower cost, effective, and secure alternatives within the available radio market." Essentially, the Army wants to ensure that the NDI will have the capability to use certain waveforms – Wideband Networking Waveform (WNW) and the Soldier Radio Waveform (SRW) specifically – at an affordable price, according the spokesman.

Army officials say that previous research and development investment in SDRs through the GMR and JTRS program created alternatives that may be more price competitive than the GMR was becoming.

Army leaders are planning to conduct a full and open competition in early 2012, aimed at leveraging mature technologies for a replacement to the GMR. The new program will manage "the evaluation, testing, and delivery of affordable Non-Developmental Item (NDI) products fielded to operational units."

Figure 1 | The Manpack JTRS radio from General Dynamics Systems is part of the JTRS Handheld, Manpack, and Small Form Fit (HMS) program.

According to the JPEO JTRS spokesman, Brig. Gen. Michael E. Williamson, JPEO JTRS told a media roundtable the NDI radios are likely to meet revised requirements at a lower cost, with key improvements in radio Size, Weight, and Power (SWaP). Competition and the Army's Network Integration Evaluation (NIE) will be used to evaluate and test the radios.

And then there were three

The HMS, AMF, and MIDS are all in various stages of production with deployment on track for next year. None have been cancelled, but system integrators on those programs are acutely aware of the cost pressures coming out of the Pentagon.

"Of course there are concerns with DoD budget cuts. The whole industry is concerned and debates and discussions are ongoing in Congress," says Joe Miller, Director of JTRS Military Radio Programs for General Dynamics C4 Systems in Phoenix. "I will say this much: As far as HMS is concerned, the Army is strongly behind it."

"The Army really doesn't have any choice but to buy these radios, as their current radios don't support networking waveforms," Miller says. The networking waveforms key to HMS include the SRW, the Sideband Networking Waveform (SNW), and the Mobile User Objective System (MUOS) waveform, he says.

On HMS "we have progressed through Milestone C and are currently under Low-Rate Initial Production (LRIP) for the two-channel Manpack and orders for the Rifleman radio," Miller says (Figure 1). "We will start delivering Rifleman units at the end of this year with Manpacks following next year, with testing an ongoing process."

Milestone C is the part of the acquisition process where entry into the production and development phase is approved.

Rockwell Collins in Cedar Rapids, Iowa, is also on the HMS variant, producing Manpack radios and implementing software infrastructure in the Manpacks to host new waveforms as they are developed, says Robert Haag, Vice President and General Manager of

Communication and Navigation Products for Rockwell Collins.

"JTRS will continue to evolve as we add capability features to it, and there will be additional international waveforms" adapted as they operate with allied troops, Haag says.

Lockheed Martin AMF

The Lockheed Martin AMF JTRS team has also been restructuring their services to be more cost effective and get through Milestone C by 2013, says James Quinn, Vice President, C4ISR Systems at Lockheed Martin Information Systems & Global Solutions in Littleton, Colo.

The Army is currently putting the AMF and HMS radio systems and their designers through NIE demonstration – to get warfighters used to technology and to test out the capabilities as well.

During the NIE held in November, the AMF JTRS system's range and capability were tested relaying voice, data, and imagery from a test bed AH-64 Block III Apache helicopter to ground forces over the SRW, according to Lockheed Martin officials.

During the exercise, an AMF JTRS Small Airborne radio in the Apache enabled pilots to communicate with six different ground elements using JTRS HMS Rifleman radios (Figure 2).

Using AMF JTRS, the Apache provided an automatic relay enabling warfighters using HMS Rifleman radios to communicate by voice and data with the Apache over long distances. Ground forces were able to markup imagery and redistribute to other users connected via the JTRS network through applications on the AMF JTRS radio, according to a Lockheed Martin release.

Lockheed Martin's AMF JTRS team includes General Dynamics, Northrop Grumman, Raytheon, and BAE Systems.

MIDS

The MIDS JTRS terminals are already in production, Haag says. ViaSat in San Diego and Data Link Solutions – a joint venture between BAE Systems and Rockwell Collins – are supplying the MIDS JTRS terminals.

The MIDS Program Office most recently awarded MIDS JTRS terminal production contracts to both companies with Data Link Solutions getting about $9 million, and ViaSat receiving more than $13 million, according to a JTRS JPEO release. The contracted work will deliver the first series of annual block cycle software updates for MIDS JTRS terminals. Block Cycle 1 will provide information assurance modernization upgrades and other enhancements.

Figure 2 | The AMF JTRS system was placed inside an AH-64 Block III Apache helicopter to test range and capability while relaying voice, data, and imagery from the Apache to ground forces over the Soldier Radio Waveform during an Army Network Integration Evaluation.

The four-channel MIDS JTRS features Link 16 capability and can also add other waveforms when needed such as the Rockwell Collins-developed Tactical Targeting Networking Technology (TTNT) waveform, Haag says. The MIDS JTRS Terminals will be used for the F/A-18E/F, the U RC-135, and the EC-130H Compass Call, according to Rockwell Collins.

TTNT – which is a tactical data link for airborne networking – was used this past summer for secure communications in the Unmanned Combat Air System Aircraft Carrier Demonstration (UCAS-D) program, Haag adds.

SDR systems already deployed

While JTRS has yet to be fully deployed, SDRs are being used by warfighters every day in the field.

Some of the most widely fielded radios today are SDRs, says Manuel Uhm, a member of the Wireless Innovation Forum board of directors and Vice President of Marketing for Coherent Logix in Austin, Texas. They include the Harris Falcon III AN/PRC-117G radios and the Thales AN/PRC-148 JEM radio, which were funded as specific JTRS development programs. Both companies developed this on their own nickel, which gave them a huge advantage in getting to market sooner than other JTRS guys, he adds.

The Falcon III AN/PRC-117G multiband manpack radios from Harris RF Communications are software-defined and provide voice, video, and wideband data communications to warfighters, according to a Harris public release. It also uses applications such as collaborative chat, streaming video, and secure networking.

The AN/PRC-148 JEM – The Joint Tactical Radio System Enhanced Multiband Inter/Intra Team Radio – is a small, lightweight, and multiband tactical, handheld radio covering the 30-512 MHz frequency range, according to the Thales website.

General Dynamics fielded the first SDR system close to two decades ago with the Digital Modular Radio (DMR) system for U.S. Navy ships. "We are in the sixth production run on the system, which was developed in the early 1990s," Miller says.

Rockwell Collins engineers are bringing SDR capability to current systems by adding a software-defined architecture to existing radios, Haag says. "We are bringing more value to the warfighter by adding capability to existing ARC-210 radios without taking more space and changing the footprint," Haag says. Essentially the ARC-210 Gen5 now has SDR capability without needing a new form factor.

"We are trying to demonstrate that you can get improvements in capability without buying new pieces of equipment, but by modifying existing radios," he says.

The Gen5 uses a software-defined, multiwaveform architecture – a version of the Software Communications Architecture (SCA). It is a form-and-fit replacement for current ARC-210 radios and also complies with National Security Agency (NSA) cryptographic initiatives.

The new ARC-210 radio will have Joint Precision Approach and Landing System (JPALS) UHF data link capability and will support insertion of Tactical Secure Voice (TSV), Integrated Waveform, Combat Net Radio, and SRW.

SDR beyond JTRS

JTRS and SDR technology essentially created a revolution – turning radios into powerful computers with an RF front end, Miller says.

In the future, the SDR system will continue to evolve along these lines and eventually adapt attributes and features of popular commercial devices such as tablets or iPads, where functionality and capability will be in the form of applications added through the software, he continues. Different applications will be uploaded, run on the SDR for specific missions and different needs using waveforms with different performance characteristics based on mission requirements, Miller adds.

Potential applications include video compression, target tracking, mosaic for video, sniper detection, combat identification, and monitoring warfighter health, Miller says.

The next evolution will be turning these radios/computers into a sensor system by adding sensors to the equipment. When each radio becomes a sensor, a diverse spatial network is created in a mobile environment, Miller says. Each warfighter with a radio becomes a node on the sensor network. These "sensors" provide greater situational awareness to the command and control elements that analyze the information, he continues.

The U.S. military is much closer to demonstrating some of these applications today, and General Dynamics is under contract to further develop some of them, Miller says. For example, Army planners are looking for more commercial solutions like Android so they can leverage the low cost of these devices while still protecting the data on the systems, he explains. A lot of companies are working on using the Android and running secure applications on its operating system, he adds.

"We have an Android-based device that integrates with the Rifleman Radio and is worn on wrist that pulls up and displays maps," Miller says.

Smartphone-like devices are definitely the future, as they are very compact and, most importantly, can run for a significant length of time on battery power, Uhm says.

Technology at the component level is beginning to catch up with SDR, which is enabling this transformation, Miller says.

SDR technology continues to evolve as it takes advantage of commercial cellular and tablet technology, Haag says. There is a lot of opportunity to drive cost improvements through new processing elements, backplane configurations, and memory cores. **MES**

U.S. Navy photo by Mass Communication Specialist 2nd Class Lewis Hunsaker

Measurement and analysis techniques for wireless systems

By Mike Donovan and Dr. Jon Friedman

Developing commercial and military wireless receivers is a challenging task, requiring engineers to understand the specification, design and implement an algorithm that can discriminate between signals of interest and spurious signals, and test the algorithms to verify they perform properly. Using MATLAB, the authors demonstrate how each of these steps can be completed using the Mode S aircraft communication standard.

Commercial and military communication standards require that waveforms adhere to rigid specifications to ensure that devices interoperate with equipment from other vendors. Wireless transmitter and receiver designs both need to adhere to standards, but transmitter design is typically a straightforward process. Wireless receiver design is a more challenging exercise, and the use of real-world test signals can significantly accelerate the design process and ensure interoperability. The tasks involved in the design of a wireless receiver include:

- Develop receiver algorithms
- Create test vectors and run tests on a PC
- Conduct laboratory tests of the design in a controlled environment
- Verify the design works with captured field data

Some of these tasks require technical computing software; others require test and measurement tools. The following discussion uses the Mode S secondary surveillance radar standard as an example to demonstrate how a unified technical computing and measurement environment enables engineers to develop more robust designs, use real-world data to verify they meet performance specifications, and confirm that they satisfy interoperability requirements.

Mode S signal details

Mode S is a transponder-based communication system used by commercial aircraft to report their aircraft identification, position, altitude, and velocity to air traffic controllers and collision avoidance systems. Transmitters on the ground send interrogations to commercial aircraft, and the aircraft respond with flight information to those queries. The Mode S standard is published by the International Civil Aircraft Organization. The standard has already been adopted in Europe and is being gradually introduced in the United States. The Mode S standard specifies details of the signal format:

- Transmit frequency: 1,090 MHz
- Modulation: Pulse position modulation
- Data rate: 1 Mbps
- Message length: 56 µsec or 112 µsec
- 24-bit CRC checksum

The message content depends on whether the specific message is short (56 µsec) or long (112 µsec). Short messages contain the message type, aircraft identification number, and a CRC checksum. Long messages also contain the altitude, position, velocity, and status. Each Mode S message begins with an 8-µsec synchronization and preamble. This information establishes that a valid message is being transmitted and enables receivers to determine when the message bits start.

Receiver algorithm design

Mode S communication is characterized by very short messages interspersed with long idle periods. In a crowded airspace, there can be several commercial aircraft transmitting multiple legacy signals in the same frequency band that Mode S uses. A Mode S receiver must reject these legacy signals as well as other spurious signals, recognize the presence of a Mode S message, and launch a demodulation and decoding process to extract the data.

Decoding a Mode S message starts with correlating the incoming signal to the Mode S synchronization pattern and comparing the result of the correlation to the noise floor of the receiver. When the synchronization pulse is present, the correlation should be well above the noise floor so that the peak correlation value can be used to calculate the start of the message bits (see Figure 1).

Each 1-μsec message bit has one of two possible bit patterns. A logical 1 is on for the first 0.5 μsec and off for the second 0.5 μsec; a logical 0 is off for the first 0.5 μsec and on for the second 0.5 μsec. If the receiver sample rate is set to 12.5 MHz, each bit will comprise either 12 or 13 samples. A simple strategy for bit decoding is to sum the magnitude of the first six samples and the last six samples for any individual bit and assign a 1 or a 0 based on the results.

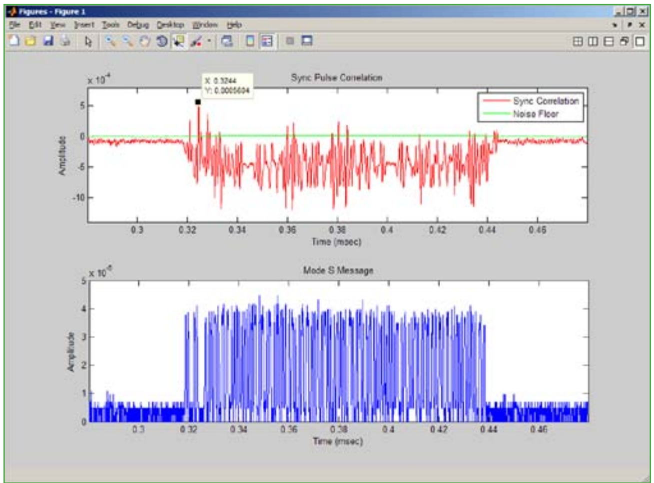

Figure 1 | Correlation of data to the Mode S synchronization pattern and comparison to the receiver noise floor.

The last 24 bits in the message are the CRC checksum. To ensure the message has been properly received, the receiver must compute the checksum for the message bits and compare it to the last 24 bits in the message. If the computed checksum matches the received checksum, the message is valid and the message type, aircraft ID, position, altitude, and velocity can be decoded.

To speed up the development and testing of the algorithm, engineers today use technical computing environments that enable them to seamlessly develop and test algorithms using both synthesized and captured data.

Algorithm testing with Mode S data

Engineers will typically verify receiver algorithms using test data from multiple sources, including:

- Data generated synthetically and formatted using the Mode S standard
- A test signal transmitted in the lab and captured by test equipment
- Real-world RF data captured from aircraft flying overhead

For example, receiver designers might start by constructing baseband data signals that match the Mode S responses to test their algorithm. They could then add impairments such as random noise to test the algorithm's robustness. This approach serves as an initial test to verify that the basic receiver processing works correctly and to determine performance boundaries, such as the minimum Signal-to-Noise Ratio (SNR) needed for reliable reception. As a next step, the designer might generate an ideal signal using a waveform generator and verify the algorithm by capturing this signal with test equipment.

Once the algorithm has been tested against an ideal signal, the design is ready to be tested against multiple Mode S transponders. Verifying interoperability is important because multiple vendors design and sell Mode S equipment. Testing with real-world signals is vital because it is easy to misinterpret the standard, which is 213 pages long, and testing against multiple designs can reveal overlooked nuances in the standard. Also, the RF environment is unpredictable and introduces many impairments, including interferers within the specified frequency spectrum and distortions introduced by transmitters in addition to complex channels with problems caused by multipath reflections, weather, and foliage.

Using modern signal and spectrum analyzers engineers can capture live Mode S data by tuning to the response frequency, setting the sampling rate, and storing the received In-Phase/Quadrature data. The recorded data can then be used to validate that the receiver design works with real-world signals.

If the algorithm is designed in a technical computing environment, then much of this part of the testing process can be automated. First, the spectrum analyzer can be controlled using script commands sent via GPIB or USB interfaces. Most front-panel controls on the spectrum analyzer can be accessed and scripted using these interfaces. Second, data from the spectrum analyzer can be imported directly into the environment. This approach provides several advantages. First, scripting ensures tests are repeatable. Second, scripting enables testers to launch lengthy tests without having to manually conduct the test process. And third, scripting can be used to automate data retrieval and eliminate the need to manually run file transfers, burn DVDs, or set up network drives.

When using MathWorks Instrument Control Toolbox, controlling and analyzing data from a spectrum analyzer is a three-step process:

Connect: Establish a network connection between a PC and the test equipment.

Measure: Set measurement parameters and send capture commands to the test equipment.

Analyze: Retrieve captured data from the test equipment over the network connection and process the data.

The testing process is also accelerated when the measurement script is developed interactively and graphically. For example, as they develop scripts, engineers can execute Standard Commands for Programmable Instruments (SCPI) instructions from the MATLAB command prompt and use the Test and Measurement Tool graphical user interface to communicate with the test instrument.

A sample test script is shown in Figure 2. The script sets up the instrument, issues the capture commands, and retrieves the data. Writing a test script does require a small additional time investment up front compared to performing the steps of a single manual test. However, as scripts are reused multiple times or employed to automate long, unattended tests, the investment is recouped many times over in time savings.

Using a spectrum analyzer and the approach outlined here, engineers can receive and decode Mode S signals from aircraft flying nearby.

Automated testing

Unifying the measurement and computation segments of this example gives an engineer designing the receiver the ability to run automated tests on an algorithm design with real signal sources. A receiver design that works well on one test data set might fail with equipment from other vendors or in different wireless environments.

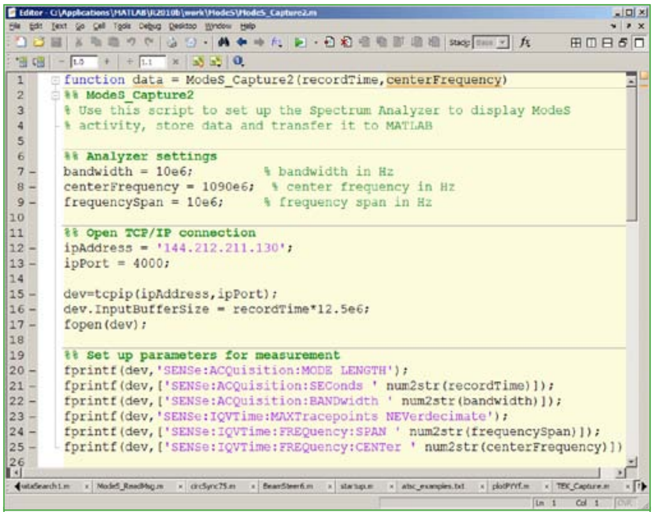

Figure 2 | A sample Mode S test script

An automated process helps engineers run tests efficiently against a wide range of test conditions and vendor equipment.

Stronger algorithms, more fully tested designs

Accessing data transmitted from real wireless sources is a key step in verifying a receiver design. A unified environment in which engineers develop algorithms and automate the collection and processing of data streamlines development. MATLAB and Instrument Control Toolbox were used to write a 300-line script to:

- Control wireless test equipment, including spectrum analyzers
- Retrieve stored data for off-line processing
- Demodulate and decode the received data

Using this approach and a unified environment, wireless engineers can access more realistic data, try out more receiver algorithms, and run more performance tests. This ultimately produces stronger algorithms and more fully tested designs. **MES**

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U.S. Air Force photo by Senior Airman Gustavo Gonzalez

If power is the problem, can GPGPU be the solution?

By Peter Thompson

The requirement for maximum processing performance has driven the growing use of GPGPU technology in a range of mil/aero applications. However, future developments in the GPU space look as if they will also address the requirement for optimum performance/watt.

General-Purpose computing on Graphics Processing Units (GPGPU) has been around for several years in the commercial domain, and has been deployed in the rugged mil/aero space since 2009. Engineers are comfortable with recasting compute problems to fit the programming paradigm, and fully rugged, conduction-cooled platforms are mature and in the field.

GPUs have already found a home with those pushing the envelope on performance and Size, Weight, and Power (SWaP). They have been deployed effectively in radar processing systems, shrinking the processing footprint for modes like Synthetic Aperture Radar (SAR) imaging and Ground Moving Target Indicator (GMTI) applications, as well as in Signals Intelligence (SIGINT) systems. Beyond this, they are naturally very effective in high-bandwidth imaging applications, such as wide-area surveillance, where hundreds of cameras are mosaicked into one and processed. Hyperspectral imaging also is a prime GPGPU application, because of the greatly increased bandwidth from sensing hundreds or thousands of bands and the dense operations for classifying hyperspectral data.

The next wave of GPGPU devices is about to hit the marketplace, and these latest devices show a new focus on power consumption. Just as with “traditional” processors, the emphasis has increasingly shifted toward performance per watt in order to enable new classes of application. Whether it is measured as GFLOPS per watt or picoJoules per instruction, and whether the technology is being applied to battery-powered night vision goggles or to DARPA-hard Exascale Grand Problems, the amount of power consumed and the amount of heat to be rejected are increasingly important. A shift in emphasis from GPU vendors reflects this and will enable new applications at both ends of the spectrum of system size.

GPU performance/watt is the new focus

When Jen-Hsun Huang gave the keynote speech at NVIDIA’s GPU Technology Conference in 2010, one thing of particular interest was that the GPU road map he showed depicted not performance, but rather, for the first time, performance per watt (Figure 1).

This is a significant acknowledgement from a market segment that until now has been notoriously insensitive to power. One of the driving forces at play is the widespread adoption of GPGPU in Petascale High Performance Computing. As an example, the current fastest supercomputer in the world today uses more than 7,000 GPUs to yield more than 2 PetaFLOPS (1,015 floating-point operations per second), but at the expense of around 4 MegaWatts of power consumption.

NVIDIA is a member of one of four consortia awarded contracts by DARPA to study architectures that can reach Exascale: an increase in performance of 1,000 (1,018 floating-point operations per second). One of the challenges is how to achieve this without an accompanying increase in power consumption of three orders of magnitude. It is becoming increasingly apparent that the mil/aero embedded computing segment will benefit from developments in this arena.

When GE Intelligent Platforms released a range of products based on NVIDIA's GT240 GPU, such as the IPN250 (Figure 2), this represented a significant sweet spot on the performance per watt curve for rugged deployment. Even the next generation of GPUs, the Fermi family, struggled to match the GT240 for efficiency. The versions that boasted more performance typically came at a significant power penalty. For example, the GT240 peaks at 385 GFLOPS with a maximum Total Dispersed Power (TDP) of 45 W, which equates to 8.6 GFLOPS per watt. The Fermi-class GF104 peaks at 590 GFLOPS with a maximum TDP of 75 W or 7.9 GFLOPS per watt. Note that here, only Single Precision (SP) floating-point operation is considered, as the GT240 does not support double precision, and embedded computing tends to be dominated by SP operation.

There are still reasons to consider Fermi devices beyond the GFLOPS per watt metric. Substantial architectural changes include:

- Improved double precision support and performance for applications that require it
- Error correcting code memory to improve reliability
- Increased shared memory size
- True cache hierarchy to ease programming complexity
- Faster context switching
- Improved scheduling
- Increased autonomy from CPU

Road map shows fivefold improvement

NVIDIA has announced plans to ship "Kepler" products starting early in 2012. Few details on Kepler have been made public other than the predicted increase in Double Precision (DP) efficiency and how that will come from a combination of architectural changes and a smaller process geometry.

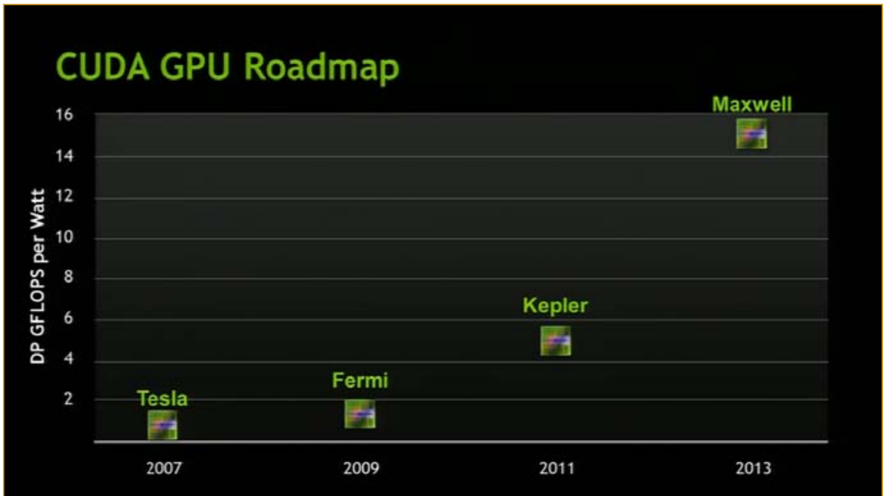

Figure 1 I NVIDIA's CUDA road map shows increasing performance per watt

Figure 2 I GE's IPN250 combines a single GT240 96-core CUDA GPU with an Intel Core 2 Duo host processor operating at 2.26 GHz and 8 GB of DDR3 SDRAM to deliver up to 390 GFLOPS of performance per card slot.

Given that Kepler offers something on the order of a fivefold increase in DP GFLOPS per watt, how will we get to ExaFLOP performance without requiring a dedicated power plant? Public presentations from senior staff at NVIDIA give some insights.

Firstly, they posit that architectures with explicit management of on-chip memory can be more efficient than their counterparts that employ hardware-driven cache hierarchies. The argument goes that distance = power when it comes to fetching operands, and that that power exceeds the power taken to do the actual mathematical operation. Even on a 28 nm process device, the difference in power taken to fetch an operand from close to the gates that will perform the operation to that taken to fetch from the other edge of the die can increase from tens of picoJoules to hundreds of picoJoules. Having to reach out off-chip to DRAM can cost tens of nanoJoules (in addition to a huge increase in access latency). This gives credence to the adage that the FLOPS are almost free; you pay to move the data.

"Having to reach out off-chip to DRAM can cost tens of nanoJoules (in addition to a huge increase in access latency). This gives credence to the adage that the FLOPS are almost free; you pay to move the data."

At Exascale, even small differences in the energy it takes to fetch an operand can have a huge impact on the system power consumption.

Secondly, NVIDIA is increasing the autonomy of the GPU and independence from the x86 CPU by integrating ARM cores into the GPU itself. This will add significant flexibility to the GPU, with new options for I/O, fused address spaces, self-scheduling, and lower latency overall. To see the effects of this, we need to look no farther than NVIDIA's Tegra devices, because that's where this technology is being developed. The current Tegra3 SoC (codenamed "KalEl") utilizes a quad-core ARM Cortex-A9 and a fifth ultra-low-power "Companion" core. Together, these ARM cores provide a dynamic range of serial compute performance, while more broadly supporting the high-performance GPU cores. While Exascale computing is a dot on the horizon, and even then will be limited to huge supercomputer installations, it can be expected that the advances that will be necessary in power efficiency will scale down to enable embedded systems also.

It is currently estimated that a GPU-based ExaFLOP machine will require 5,120 nodes and consume 15 MegaWatts. This equates to around 66 DP GFLOPS per watt. Contrast that with today's 2 DP GFLOPS per watt, and this starts to indicate that NVIDIA does indeed have a path to Exascale that matches the Fermi/Keplar/Maxwell curve on the road map.

New techniques help with heat dissipation

Even if the promised performance per watt improvement from Fermi to Kepler holds true, it is possible that, with the process shrink from 40 nm to 28 nm that is widely expected, thermal density may increase. As a die shrinks, the surface area from which waste heat is to be extracted reduces as the square of the reduction in feature size. This makes the extraction of the heat increasingly difficult.

However, there are several innovations that are starting to make their way from the laboratory to the field that will help to alleviate this issue. Thermal ground planes take the technology from heat pipes that are commonly applied to commercial electronics, and, by using innovative designs and constructions, allow it to be applied in environments with high shock and vibration levels – even negative-*g* forces. By applying such devices to conduction-cooled boards, the thermal path from die to heat frame can be much improved.

The next link in the path that heat must traverse before ultimately being dispersed to the environment is the wedgelock. This interfaces the heat frame to the chassis and forms the conducting interface by expanding when the screw mechanism inside is torqued. By reworking the construction of the wedgelock with new materials, the efficiency of the heat transfer can be increased.

Improving the heat path not only means that devices with higher power dissipation than previously could be handled may be used; just as important, by maintaining a lower maximum die temperature, the long-term reliability of the device can be improved.

New applications enabled

Early adopters of GPGPU technology in the mil/aero space focused on what it could do in terms of raw performance. As its potential becomes better understood, however, designers are looking to broaden the range of applications in which it can be deployed. This, in turn, is putting the spotlight on the performance per watt characteristics of GPUs. The good news is that manufacturers like NVIDIA are acknowledging this, and developing future generations of products that deliver not only optimum performance, but also significantly improved performance per watt. **MES**

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U.S. Army photo by Sgt. Travis Zielinski

Meeting the military challenge: Designing for wide temperature range systems

By Dr. Qi Chen

Designing embedded systems for wide temperature range rugged applications requires careful attention to detail and consideration of many aspects. Only by utilizing a comprehensive design methodology will successful implementations be achieved.

For many embedded applications, particularly those in military transportation, or where systems must be operated in harsh outdoor environments, a wide operating temperature range of -40 °C to + 85 °C is typically expected, and this can be a challenging requirement to meet.

To achieve such a rugged system specification, the design needs to take account of many special details, starting at the circuit level and also encompassing component selection, thermal design and PCB layout, and design verification testing and life-cycle management, to name just a few. It will be seen that many factors need to be considered before a successful system can be realized.

Components matter

Selection of major components is an important factor, and all the active components, such as the processor chips, memories, and regulators, need to use appropriate industrial temperature grade parts to ensure operation within specification at the temperature extremes found in wide temperature range applications. Less widely considered is that all passive components too need appropriate specifications, and resistors, capacitors, and crystals all need to be carefully selected.

Resistors, for example, need to be chosen so that they meet the tolerance requirements for resistance value across the full temperature range, and so that their power dissipations are not exceeded. This is a particularly important consideration for resistors that require accurate values but must be placed near other hot components.

Capacitors are used in large numbers in embedded designs, mostly for power supply smoothing and decoupling active components. High value bulk capacitors are needed to smooth supply rails, and electrolytics are typically used in general-purpose designs because they provide a high capacitance value in a small physical volume. However, wide temperature range system designs generally need to avoid use of electrolytics because these types of devices are not solid-state and contain gel-like materials internally. These materials can potentially change properties over time when operated at temperature extremes, partially drying out or even failing with extended use at high temperatures.

Solid-state ceramic capacitors are therefore the best choice for capacitors used in wide temperature range rugged applications. There are a number of ceramic materials for capacitors, and for these applications it is preferable to only use materials such as NPO or X7R, which have a low temperature coefficient, meaning that the change in capacitor value with temperature over the full operating range is relatively small. Standard materials such as Y5V can vary by as much as -80 percent/+20 percent, whereas an X7R variation is much lower at only ±15 percent, and NP0 has effectively no significant variation, being a very small ±30 ppm/C.

Stable capacitance values are particularly important in any circuits where the capacitor value is a carefully selected design parameter. Examples of this include filter circuits in regulator control loops and clock and timing circuits. Although these low-temperature-coefficient ceramic

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Choosing low-temperature-coefficient components also applies to clock circuit crystals, which should, for example, be specified to be only 20 ppm variation. This ensures that clocks do not change frequency with temperature in any significant way that would affect system operation. This could otherwise lead to problems at the system level, which may only occur at temperature extremes under certain conditions where clocks unexpectedly drift too far away from their nominal frequency.

Thermal design is key

To reduce internal sources of heat in the rugged embedded system, it is much preferred to use switching regulators in the power section instead of linear or LDO-type regulators. Switching regulators are more efficient, 90 percent being typical, whereas LDO efficiency depends on the voltage drop and current flowing and can be very low in comparison. Depending on the voltage drop across the regulator, 50 percent efficiency would not be unusual. The higher efficiency of the switching regulator compared to an LDO means that the switching regulator therefore produces much less excess heat. Even though a switching regulator is used, it should also still be implemented so that the design has been tuned to be as efficient as possible to further minimize any excess heat. This is particularly so at high power load conditions of 10s of Amps when the CPU is drawing maximum power.

A wide temperature range embedded rugged system needs to be designed so that all aspects of heat removal from all the heat generating components are considered. Usually the processor is the main heat producing part, but chipset and regulator parts also can generate significant amounts of heat. The processor and chipset should therefore be chosen to be as low power as possible, while still providing for the application processing requirements, and be verified to operate over the temperature range required. The heat removal from the back surface of the die at the top of the processor package is a key part of the design; a CNC-machined aluminum heat spreader is a good solution to take heat off the board and transfer it to the case, which is itself designed to be a heat sink. The heat spreader can also be used to touch most of the other main heat generating components on the PCB, such as parts of the power section, conducting their heat away from the board to the exterior heat sink surfaces of the case as well. Fans contain moving parts and are therefore vulnerable to wear and eventual failure. Although airflow from fans is very effective to remove heat from components, fanless designs are preferred because they have much higher reliability. Fanless systems are possible to achieve by factoring in careful thermal design considerations.

PCB layout and design

Effective PCB layout is also a key aspect for wide temperature range systems. It is necessary to ensure that hot components are both distributed over the PCB to avoid creating hotspots and also that these hot components are not too near to other heat sensitive components such as clock crystals. Also the PCB's metal layers can be designed where necessary so that they conduct heat (or not) in a controlled way from one part of the PCB to another. In short, the PCB, heat spreader, and case need to be designed as one overall thermal system.

PCB materials are chosen so that they have a high glass transition temperature (Tg). This is the temperature at which the board material starts to physically deform, and at the maximum ambient operating temperature of + 85 °C, all parts of the PCB are designed to be well below the maximum temperature that the PCB itself can handle before deforming. Careful control of heat generation and heat flow are therefore all part of the design process, and they are not afterthoughts added later. By careful design of the PCB, heat spreader/heat sinks, and case, it is possible to achieve an optimal thermal solution that is very reliable in operation at all temperatures within the operating range.

Design verification is vital

Once a system design has been generated using suitably chosen components and the thermal design has been completed, the next step is design verification. This is a key step in proving that the design as a whole meets the specification requirements. A number of demanding tests are used, which are designed to stress the system in different ways to expose any weaknesses. For wide temperature range systems, long-term testing involving extended operation at -40 °C and +85 °C is performed to ensure that the basic specification is met. For embedded systems, a boot-up test is particularly important and is performed a large number of times at all temperatures including the extremes. Thermal shock testing is also used, where the temperature is rapidly ramped from -40 °C directly to +85 °C, generally including both normal operation and multiple boot-up tests during the temperature ramp. Any failures in these tests are fully investigated and the design corrected where needed.

Once design verification is completed, there are further tests that can then be performed during production on boards and systems before delivery to customers. At Arbor Technology, for example, we perform vibration stress screening according to MIL-STD-781D task 401 on production boards to eliminate any that have assembly defects that may show up later during operational life. Figure 1 is an example of such a wide temperature range board: The Arbor EasyBoard-841E has specific design features included for applications such as external environments on vehicles, and is specified to operate over a -40 °C to +85 °C ambient temperature.

Product life-cycle management

For wide temperature range and high-reliability applications, a long product life cycle is a key element. To control and maintain quality and meet specifications at all times during the life cycle of the product, the manufacturer needs to pay particular attention to products that go

Figure 1 | The Arber EasyBoard-841E wide temperature range rugged board

End-Of-Life (EOL) during that time. Components that go EOL must only be replaced by compatible ones that meet the same specification, and the design verification step needs to then be repeated. Also a replacement component generally needs to be a true drop-in, even with the same footprint; otherwise the thermal environment may change because of needing to make changes to the PCB layout. This level of detailed Bill-Of-Materials (BOM) control therefore needs to extend to cover all components in the design, including capacitors and resistors, as well as the more obvious large chips.

Consistent application of design methodology

Achieving a wide temperature range embedded system design requires careful attention to detail at all stages of product design, from component selection to thermal design, through verification testing, and even into maintaining BOMs over the product life cycle. Design success is therefore a result of methodically applying a consistent integrated design methodology that attends to all these factors. **MES**

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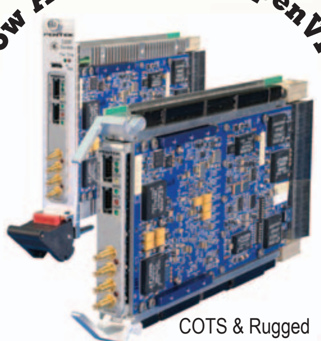

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Protect aircraft subsystems with optimized TVS devices

By Kent Walters

Lightning protection is becoming increasingly important as military aircraft adopt carbon-composite airframes and carry a growing array of fly-by-wire avionics equipment. Meeting the latest stringent lightning-protection standards requires careful selection of Transient Voltage Suppressor (TVS) devices.

The aerospace and defense industries have created standards for protecting onboard military avionics systems from lightning strikes. Few off-the-shelf Transient Voltage Suppressor (TVS) components can meet the latest surge specifications established by two of the top aviation standards bodies, and poor thermal performance has led to very high junction temperatures and impaired performance or failure. New TVS construction avoids these problems by significantly reducing junction-to-heat-sink thermal resistance and handling multistroke test sequences with minimized damaging heat accumulation in the region of the diode (p-n) junctions.

The lightning problem

While aircraft lightning strikes are not uncommon, they rarely cause problems. When an all-metal aircraft is struck by lightning, its skin becomes part of the bolt's conduction path. The ionized gas channel briefly attaches to the structure at two or more points, and the metal skin acts as a Faraday cage. Current flows over the structure's outer surface, and although induced fields inside the aircraft are not eliminated, they are at least manageable.

Lightning protection has become more important with the proliferation of fly-by-wire architectures that carry primary flight control commands over an aircraft's data bus and power wiring. Meanwhile, the commercial, aerospace, and defense industries are increasingly using carbon composites rather than the traditional aluminum alloy airframe to reduce weight while increasing structural strength. Significant skin areas on aircraft such as the Airbus 350 and 380 and the Boeing 787 are now fabricated using carbon composites. These materials approach the lightning-protection performance of traditional metal airframe materials but offer less shielding for the flight systems they enclose than do their metal equivalents.

Both metal and, to an even greater degree, carbon-composite airframes require optimized TVS components to adequately protect them from lightning strikes. Without adequate TVS protection, these strikes can damage sensitive electronic components when their maximum rated voltages or power ratings are exceeded.

Testing lightning tolerance

The American Radio Technical Commission for Aeronautics (RTCA) and European Organization for Civil Aviation Electronics (EUROCAE) defined the RTCA/DO-160E and EUROCAE/ED-14E (as well as ISO-7137) harmonized standards for the lightning-related interference levels that both metal and carbon-composite airframes must tolerate in commercial and military applications. DO-160 mandates that avionics subsystems survive exposure to direct strike pulses, as well as those caused by the transient electromagnetic field induced by each lightning strike. The

U.S. Air Force photo by Senior Airman Corey Hook

specification covers strike pulses in single-stroke, multiple-stroke, and multiple-burst sequences. The DO-160 standard specifies multiple transient waveform parameters including amplitude, rise time, decay time, number of repetitions, and repetition rate.

Detailed analysis shows that a typical negative strike comprises between one and 11 separate strokes up to a maximum of 24. These are thought to represent discharge of separate areas of charge occurring at intervals of approximately 60 milliseconds. An aircraft must tolerate as much as 640 V in the first stroke and 320 V in subsequent strokes for cable bundle tests in DO-160, and as much as 1,600 V for a single stroke.

The TVS circuit arrangement shown in Figure 1 helps protect the signal lines within and between avionics subsystems against transients induced by direct lightning strikes. It is also designed to protect terminal and interface equipment from transients that are conducted to these signal lines from other interface equipment in the aircraft.

Transients that appear on the interconnection wiring due to direct or induced effects must be diverted to ground by TVS devices before they can enter and disrupt terminal equipment at each end of the connection. The induced effects are capacitive or inductive coupling from transients with very fast rise times (expressed as di/dt or dv/dt, which refers to the rate of change in current or voltage, respectively).

Avionics TVSs are invariably semiconductor devices such as p-n junction Avalanche Breakdown Diodes (ABDs), which excel at clamping compared to other types of shunt-protection devices. ABDs offer greater efficiencies in lower clamping voltage than Metal-Oxide Varistor (MOV) devices; for instance, ABDs typically have a clamping voltage ratio (V_C/V_{BR}) of 1.35 compared to a clamping voltage ratio of 3 for MOVs. MOVs also can be subject to degradation with repeated transients, despite the individual transients being within their maximum ratings. To handle transient levels specified for lightning surge protection, TVS devices take the form of a single-diode die or stacks of series-connected diode dice for high-power devices.

Solving the thermal dissipation challenge

Due to their construction, many TVS devices do not allow internally dissipated heat to escape quickly enough to maintain junction temperatures below the semiconductor device's maximum operating range. It is important to fully understand TVS data sheet parameters and how they are affected by device construction.

One data sheet parameter is Peak Pulse Power (P_{PP}), which is specified in terms of randomly occurring events separated by long enough intervals that no heat buildup occurs. Some data sheets refer to an interval between surge events and provide a much lower DC power rating than the specified peak power rating. In these cases, DC conditions should be specified with heat-sinking arrangements to manage steady-state conditions. By comparison, heat sinking is regarded as irrelevant for short (1 millisecond or less) infrequent transient events that conclude before heat can reach the TVS exterior. Developers must carefully interpret comparative data sheet information using identical conditions.

Thermal management becomes relevant for extended, rapid-repetition rates of pulse events – anything with a duty cycle of applied, repeated surges where the average calculated power from that duty cycle exceeds its DC power ratings,

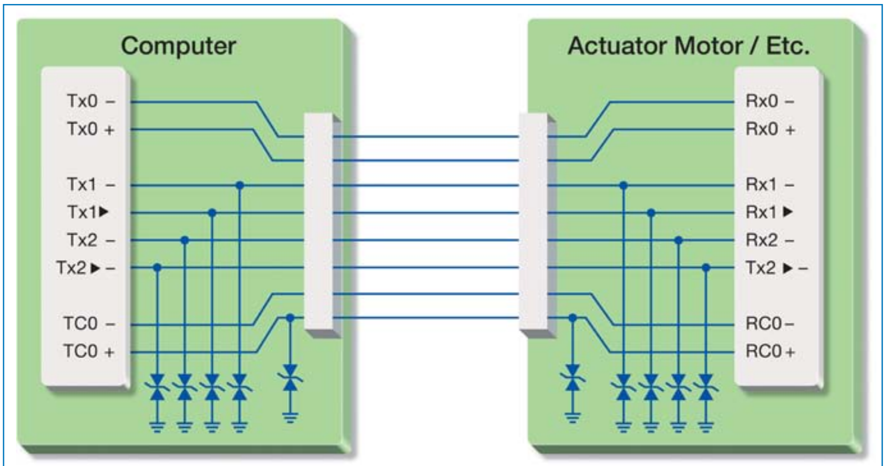

Figure 1 I A typical circuit involving TVS protection shields avionics equipment from transients caused by lightning strikes.

including any DC power heat-sinking requirements. The issue is cumulative heating effects. Developers might assume that robust heat-sinking arrangements are in place even if they aren't explicitly defined based on how the specifications are expressed in the context of controlled temperatures measured at the case, lead, or endcap.

It is important to understand that TVS devices normally operate at very low power, with very low self-heating effects until a transient occurs. This helps the TVS unit optimize transient performance and avoid possible temperature derating from its own self-heating effects if, for example, it were to be used as a Zener diode or for continuous voltage regulation where power is continuously dissipated.

Other key TVS data sheet parameters include the clamping voltage (V_C), maximum working or standoff voltage (V_{WM}), and standby current (I_D) for the leakage current at V_{WM} where the TVS normally operates before a transient occurs. With low-standby currents, TVS devices are simply idling at very low power between any randomly recurring surge events for normal operation.

The pulse shape used to define TVS device performance and test its response is typically a transient with exponential rise and decay waveforms. Because different time constants apply to rise and decay curves, a typical rating might be 130 kW at 6.4/69 microseconds. This means the device can safely dissipate a transient that peaks at a power level of 130 kW in a pulse shape that rises to its maximum in 6.4 microseconds and decays from its peak to the 50 percent level in 69 microseconds. In the case of longer pulses, the peak power value is derated to ensure that internal p-n junction temperatures do not become excessive.

At this point, TVS device construction must be considered to guarantee effective thermal dissipation. One fabrication method is an axial-leaded design. For high-power TVSs, several semiconductor dice can be stacked to achieve the required standoff voltage characteristics. This will achieve greater P_{PP} capabilities for the same Peak Pulse Current (I_{PP}) during the surge event, at which time voltage across a diode exceeds a specified value in avalanche breakdown and starts to clamp or limit the transient voltage.

However, the axial-leaded construction with stacked dice affords minimal opportunities for mounting devices directly on a heat sink to improve thermal dissipation. The thermal path starts where heat is dissipated in the stack of diode dice and continues by conduction along the leads and by convection through the casing. A relatively high thermal resistance from (p-n) junction to leads or ambient can be expected, particularly from multiple p-n junctions in the center of a stacked die design within a TVS package.

Alternatively, the dice can be assembled in a surface-mount stack, with the exposed base contact pad serving as both electrical and thermal contact. While thermal conductivity is efficient from the lowest die to the substrate, it deteriorates for higher dice. The thermal path from the top is also poor, as the last diode can only be connected to the second electrical terminal by a bond wire or small clip.

In the DO-160 multiple-stroke transient waveform, one peak transient is followed by a train of pulses peaking at 50 percent of the original peak level within 1.5 seconds. For the axial-leaded design and the surface-mount stack, the effective P_{pp} derating for these rapid multiple strokes will be substantially greater than specified for widely spaced, randomly recurring pulses. Heat will accumulate within the semiconductor device stack and won't efficiently diffuse to the heat sink or to ambient within the pulse train's timescale. This can be particularly difficult in multiple strokes where intervals can be as short as 10 milliseconds.

Optimizing thermal performance with a new TVS structure

Figure 2 shows a TVS construction that avoids the aforementioned limitations. In this example, Microsemi's PLAD plastic device employs only one or two semiconductor die of large area (depending on P_{pp} rating) connected to a large contact/thermal pad. The top contact is formed by a copper clip rather than a wire bond. The clip exits the package and acts as the second electrical contact to provide an additional thermal path. The junction-to-heat-sink thermal resistance of this structure is 0.2 °C/W, which minimizes damaging heat accumulation near the p-n junctions during DO-160 multistroke test sequences.

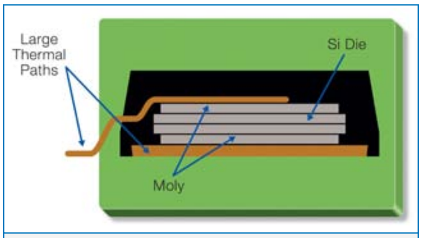

Figure 2 | Next-generation TVS construction avoids the limitations of earlier approaches by employing only one or two large area semiconductor die directly connected to a large contact/thermal pad.

Joining techniques for bonds between the semiconductor elements and contacts relieves mechanical stresses associated with any heating that occurs during the transient event. Devices can be fabricated in a sub-3.3 mm profile and feature a low-inductance current path to further improve lightning test device response. This current path is necessary to reduce inductance during a high-current transient with a fast rise time.

High magnitude of di/dt (the rate of change in current) will result in a voltage overshoot (expressed as v = Ldi/dt) beyond the clamping voltage of the TVS device. These parasitics will compromise clamping voltage performance and efficiency when used as a parallel shunt path across sensitive components needing protection.

Safer skies

The proliferation of fly-by-wire systems in military aircraft featuring carbon-composite skins has led to more robust lightning-protection standards that are difficult to support using traditional TVS constructions. New packaging techniques significantly improve thermal performance and enable TVS devices to meet today's demanding, multiple-burst surge-protection requirements. **MES**

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U.S. Army photo by Rich Bartell

Case study: Ruggedizing Cisco Ethernet switches for the military

By Mike Southworth

To meet the military's requirements for computing technologies that are cost sensitive yet extremely rugged, commercial products can be enhanced for harsh-use applications. The following case study describes how the Cisco IE-3000 switch was ruggedized for use in demanding military IP networking applications.

With military customers seeking the most robust yet economical computing systems, a "ruggedized" commercial product can often be the best solution to meet the needs of a specific military application. The terms "rugged" and "ruggedized" are often used to describe electronics capable of enduring harsh environments; however, there is a strong distinction between the two terms that indicates how a product for military use was created.

"Rugged" systems are products that are designed from the ground up to meet the requirements of specific harsh environments. Conversely, the term "ruggedized" refers to a commercial product that was not originally intended for harsh-use application, but was enhanced to endure airborne, ground vehicle, and/or shipboard deployments. The following case study examines how Parvus engineers ruggedized Cisco Systems' commercial IE-3000 switch for use in demanding military IP networking technology refresh applications.

Cisco dominates military's networking infrastructure

Cisco CEO John Chambers reported earlier this year to Fox Business that the networking giant has more than 70 percent market share in the public sector. The pervasiveness of Cisco technology and its IOS software in the government arena makes this networking technology an ideal platform for ruggedized products. Additionally, Cisco is credited with helping to define many of today's networking standards and protocols, actively contributing to the standards committees within the Internet Task Force, IEEE, and other groups. As a consequence, with the government's widespread adoption of Cisco products and its comprehensive feature set, military contractors are increasingly seeking Cisco-based rugged computing technologies for deployment in tactical military applications onboard air and land vehicles (Figure 1).

From the military's perspective, adopting ruggedized Cisco switches and networking products provides a cost-effective method for implementing the latest networking technology that meets stringent environmental standards. Also, deploying ruggedized Cisco products reduces time to deployment on the battlefield, as many military personnel are trained to operate Cisco's network management software.

One of Cisco's latest Ethernet switches, the IE-3000, recently proved to be an ideal ruggedization candidate for military use, as this switch was designed for industrial Ethernet applications, including factory automation, energy and process control, and Intelligent Transportation Systems

(ITSs). As its intended commercial use already exceeded traditional commercial environments, the Cisco IE-3000 switch included extended temperature and enhanced shock/vibration and surge ratings not typically offered by commercial networking gear.

Optimizing the IE-3000 to meet EMI standards

Although the IE-3000 is considerably more rugged than the norm for a commercial product, military-level requirements dictated that engineers further optimize the switch by making mechanical enhancements for ingress protection against dust, water, and EMI (Table 1). The EMI compliance standard required for military use includes MIL-STD-461 for radiated and conducted emissions and radiated and conducted susceptibility.

Ruggedizing the IE-3000 to meet this rugged EMI standard required protection against input voltage inversion, voltage surges, and overvoltage spikes in accordance with MIL-STD-704 and -1275. This was accomplished through the implementation of a reverse voltage/overvoltage protection circuit. Engineers also implemented several improvements, such as designing a sealed enclosure with good EMI gaskets and creating proper test cables. Moreover, proper grounding techniques and good bonding between chassis surfaces were critical in creating an enclosure to act as a faraday cage. Since external power leads are typically unshielded in test and application, they can be the single largest point of noise and susceptibility. By including a well-designed filter at the point where power enters the system, the ruggedized IE-3000 complies with EMI requirements as the filter prevents internal noise from exiting the system and protects sensitive electronics from external noise that otherwise might enter the system.

Connectors and cables: Ensuring stability for possible points of failure

Like many commercial products, the IE-3000 includes RJ-45 network connectors. Although adequate for the IE-3000's original purposes, these RJ-45 connectors are notoriously prone to failure under extreme vibration and do not provide ingress protection against dust and water. Parvus engineers removed and replaced them with locking headers that ultimately terminated with circular MIL-DTL-38999-style connectors that not only protect against dust, water, vibration, and shock, but also bring ports to the outside world.

Although a cableless design is optimal for rugged conditions, when ruggedizing an existing commercial product that includes cables, not all cables may be eliminated; thus, additional steps need to be taken to ensure stability. Since the IE-3000 contains some cabling, engineers leveraged rigid flex circuits and board-to-board interfaces where possible and implemented cable braiding, tie-downs, and other strain-relief features to maximize reliability and prevent the cables from disconnecting or being severed in vibration or shock.

Ruggedizing components to survive environmental extremes

To further ruggedize the Cisco IE-3000, additional techniques were implemented to stabilize the components during shock and vibration. One such technique

Figure 1 | Humvee: Installing ruggedized Cisco-based technology in military vehicles provides a cost-effective means of deploying a networking technology that can endure the world's harshest conditions.

	Ruggedized switch	Commercial switch
Target applications	Helicopter, UAV, wheeled vehicles, tracked vehicles, aircraft	Intelligent transportation systems, factory floor, energy/process control
Thermal (operating)	-40 °C to +71 °C (-40 °F to +160 °F)	-40 °C to +70 °C (-40 °F to +158 °F)
Thermal (storage)	-40 °C to +85 °C (-40 °F to +185 °F)	-25 °C to +85 °C (-13 °F to +185 °F)
Cooling	Passive, integrated heat spreaders	Passive, integrated heat sinks
Enclosure	Sealed aluminum extrusion	Ventilated plastic and sheet metal box
Shock (operating)	40 *g* – MIL-STD-810G	20 *g*
Shock (storage)	75 *g* – MIL-STD-810G	30 *g*
Vibration	Jet-helo-tracked vehicle ranges – MIL-STD-810G	Industrial ranges
Connectors	MIL-DTL-38999	RJ-45
Dust ingress	Dusttight (similar to IP6X) – MIL-STD-810G	IP2X (solid object >12.5 mm i.e. fingers)
Water ingress	Water immersion up to 1 meter (similar to IPX7) – MIL-STD-810G	IP0X (no water protection)
MIL-STD power	MIL-STD-1275/704 compliant	Not supported
Conformal coating	Conformal coated PCBs	No
EMI/EMC	MIL-STD-461F CE102, CS101, RE102, RS103	IEC61000, EN 50081, EN 50082-2, EN 61131-2, EN 61326-1

Table 1 | Table comparing metrics between the commercial Cisco IE-3000 switch and the ruggedized version

includes potting. Potting can be performed by completely encapsulating an electronic device or by staking it down, to provide protection against shock and vibration. For ruggedizing the IE-3000, potting was an essential procedure, as it ensures security of sensitive designs and creates a barrier against moisture, fungus, dust, and corrosion. By enhancing circuit reliability by eliminating leakage from high-voltage circuits, potting protects against voltage arcs and short circuits and prevents the formation of tin whiskers.

Potting materials come in a multitude of varieties, the selection of which is determined by requirements including thermal, outgassing, electrical and thermal isolation or conduction capabilities, and manufacturing application requirements. The selection of the correct potting materials is a key engineering decision as it can determine the proper functioning of system components.

As a final step, engineers applied conformal coating material to the IE-3000's electronic circuitry to protect it from moisture, dust, chemicals, and temperature extremes. This process improves and extends the working life of the board and helps ensure safety and reliability. These coatings "conform" to the contours of the board and its components, creating a thin protective layer that is both lightweight and flexible. For circuit boards that are not conformal coated, extreme environmental conditions could cause corrosion, mold growth, and current leakage, resulting in board failure. Taking extra precautions to ensure that the board circuitry can endure harsh conditions is paramount in designing and building a ruggedized computing system that will last through the life of the product.

Thermal management techniques ensure rugged performance

With heat issues often credited as the largest contributor to system failures, ruggedizing systems to meet these thermal challenges is a critical step. Thermal management for defense applications has always been a challenge because of

"By enhancing circuit reliability by eliminating leakage from high-voltage circuits, potting protects against voltage arcs and short circuits and prevents the formation of tin whiskers."

the high operating temperatures of the latest processors and dense packaging needed for environmental ruggedness. Cisco's standard IE-3000 switch relies

Figure 2 | A look inside the DuraNET 3000 shows various ruggedization techniques such as conformal coating and cable braiding.

on internal heat sinks and a vented case with passive airflow through the case to cool the unit. However, relying on convection cooling only inside a completely sealed box would have severe limits, so Parvus incorporated conduction-cooling techniques to maximize the heat transfer, while the unit still remained fanless and passively cooled.

To reduce weight and speed the system's heat transfer rate, engineers removed all of the standard Cisco finned heat sinks and replaced them with heat spreaders, which are conduction-cooling mechanisms. The inclusion of heat spreaders, thin sheets of metal incorporated on top of a device to help dissipate heat, significantly reduced thermal issues inside the IE-3000. These heat spreaders route heat through an internal rail/truss system that supports all of the circuit card assemblies from shock/vibration and dissipates the heat to the aluminum enclosure that incorporates finning on the outside to maximize surface area for cooling.

Further identifying any potential thermal management issues, engineers used thermal modeling software to analyze potential cooling issues, ensuring the new thermal devices included in the ruggedized Cisco IE-3000 iteration – called the "DuraNET 3000" – would meet specific military standards. Infrared imaging cameras were also used to locate any hot spots or thermal concerns. By running a variety of analyses, engineers quickly determined where potential points of failure could exist when subjected to the extreme temperatures encountered by the military.

Bringing it all together

As evidenced by the creation of the DuraNET 3000, the process of ruggedizing a commercial product for military use is no small feat. However, ruggedized products can take advantage of the technological advancements made by the world's leading network manufacturers and, when combined with proven ruggedization techniques, offer a robust, cost-effective computing choice engineered to meet today's military requirements. **MES**

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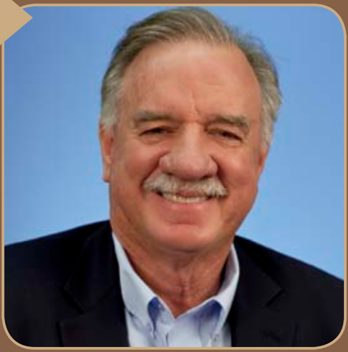
Interview with Glenn Beck, Network Products Division, Freescale Aerospace and Defense/Single Board Computing Market Segment Manager



Editor's note: An oft-posed question in the military embedded space the past couple of years has been: Will Freescale ever bring AltiVec back? That question was recently answered when the company announced its AMP Series featuring … reinstated AltiVec. Managing Editor Sharon Hess interviewed Glenn Beck, Market Segment Manager for the Network Products Division, Freescale Aerospace and Defense/Single Board Computing Market, in the following Q&A. Key want-to-knows surrounded AltiVec – why the disappearing act, and is it around to stay? – in addition to how Freescale plans to help mitigate the industry's power-versus-performance paradox. And there's a little about systems security, too. Edited excerpts follow.

What is the focus of the division you work for at Freescale?

BECK: I'm with the Network Products Division. We have responsibility for Power Architecture technology, where we build processors primarily for the networking and telecom marketplace as well as the general industrial marketplace. Because our products offer specific blends of performance and energy efficiency, Freescale's processors are well established within the aerospace and defense markets as well. Whether it is in flight controllers, graphic displays, or radar imaging, we're involved in it all.

I understand that Freescale recently introduced its new QorIQ AMP Series. Aren't they the processors with AltiVec technology reinstated?

BECK: Yes. We created a family of processors called QorIQ communications platforms, beginning with the P Series family, based on 45 nanometer process technologies. We have products that range from less than 5 W to a maximum of 30 W. Just recently, we announced the new QorIQ AMP Series products, based on 28 nanometer technology. This new family of QorIQ AMP processors is a continuation of multicore processing platforms introduced as QorIQ communications platforms. Clearly, the use of many-core microprocessors is how the industry can deliver more performance within embedded power envelopes. Freescale's trust architecture is also designed into the AMP processors, providing the ability to securely boot up the device, provide domain separation, and detect external threats to one's system. In addition, the AMP series has reintroduced AltiVec technology, which is available on our new e600 core. AltiVec is used in aerospace and defense applications as a signal processor within a control/communications processor. It is well adapted in radar and graphics display imaging – basically, in any signal processing application.

Okay, let's talk AltiVec technology for a moment, which has been a hot topic in a lot of the discussions I have been sitting in on. AltiVec went away for a while, and now it's back in this AMP Series processor. What was the impetus?

BECK: Right, so everybody remembers that AltiVec technology was first introduced in the MPC7400 series processors. That core later became known as the e600 core when it became part of a System on Chip (SoC) platform. The first introduction of the QorIQ family used the e500 core, which didn't include AltiVec technology. There is no doubt that the aerospace and defense market has had strong adoption of AltiVec technology for many years, and frankly it was missed by this market. But over the past three to four years, we have seen an increased demand and requirement for SIMD-like performance in other markets outside aerospace and defense. Like a lot of companies, we are market- and customer-driven and we began to see a need for AltiVec in the telecom, networking, video surveillance, and medical imaging spaces, to name just a few. As those appeared, we knew it was appropriate to bring this technology back to the QorIQ family of processors. That reintroduction has occurred in the recently announced QorIQ AMP T4240 product.

Looking forward, do you think all of your processors will have AltiVec on them?

BECK: As far as I can see for the foreseeable future, there is no reason for us to not include the technology in our QorIQ products. In fact, I think we expect constant improvements in the future.

Are there any specific road maps for improving AltiVec?

BECK: None that I can speak to at this time; however, many choices will be available to customers. If you remember, we first introduced AltiVec in the MPC7400. Then in about a year and a half, there was an MPC7410. And in another year and a half, there was an MPC7445, and on and on until we came to MPC7448. So about every year and a half we would have a new device with AltiVec technology incorporated, delivering ever-increasing performance. With the QorIQ AMP series, one can expect to see a number of devices across the T1 to T5 series over the next 12 to 24 months. This will provide customers more choices across a broad range of power, performance, and cost and greater alternatives for all kinds of applications.

> Earlier you mentioned the AMP Series facing challenges of more performance in power envelopes and security issues. Let's address those.

BECK: Whether it is the soldier on the ground or in the plane in the sky, the amount of voice, data, and video processing required is rising astronomically. In addition, more systems are becoming unmanned, whether they are aerial or ground vehicles. These UAV systems are requiring ever-increasing sensing capability for growing data analysis. The result is a need for more autonomous real-time decision capability at the point of data collection. This translates directly to the need of more processing capability within very demanding power (heat) envelopes.

Classically, the way we have provided better performance is by decreasing the size of transistors, which means you're able to switch transistors quicker and therefore deliver more frequency. We complement this with increasing performance through system functionality. We have moved from PCI at 66 MHz to PCI Express interconnect at 1 and 2.5 GHz and PCI Gen2 at 5 GHz and are moving from DDR1 to DDR3 memory controllers. All of those help system performance. I do not know about you, but it seems this transition has occurred in such a short period of time. At Freescale we design SoC microprocessors that balance performance across cores, memory, and I/O subsystems in a single device at particular embedded power envelopes (Figure 1). This platform strategy provides customers alternatives to get the maximum performance for their applications.

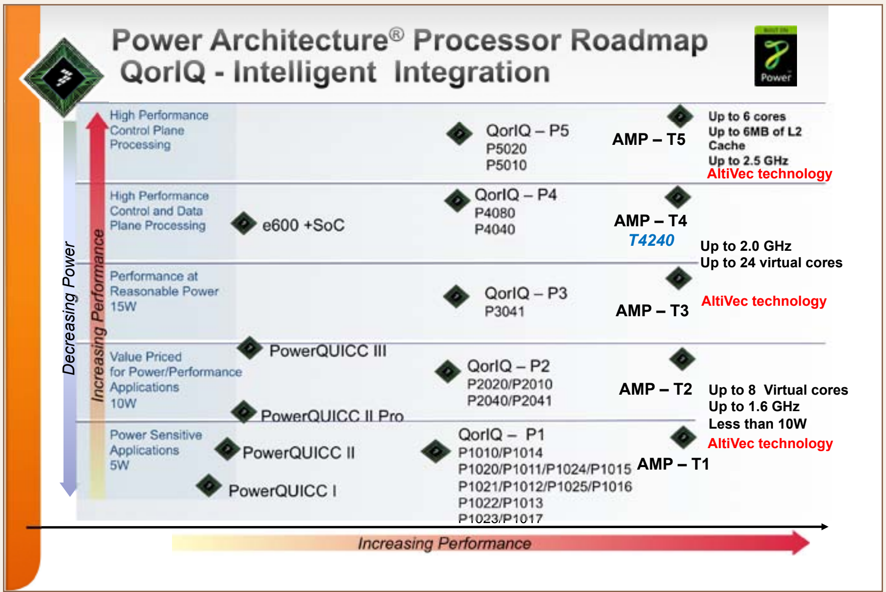


Figure 1 | Road map depiction for Power Architecture devices

The other way you increase system performance is by increasing the frequency and the number of cores. Of course, the challenge associated with this is increased power and heat. We designed the QorIQ platforms devices within designated power envelopes. For example, the P1 family is a 5 W envelope, P2 is 10 W, P3 is a 15 W envelope, and P4 and P5 devices are 30 W envelopes. All these P series processors are 45 nanometer products.

> Those are the original QorIQ processors, but can you give a technical example of this improved power envelope for the AMP Series?

BECK: As a design philosophy we balance SoC devices that utilize cores, hardware accelerators, memory, and I/O subsystems. The T4240 uses the new e6500 Power Architecture core. This 64-bit core is dual threaded, with L1 and L2 cache and also contains the 128-bit AltiVec unit. These cores connect inside an SoC platform via a coherency fabric that allows us to create point-to-point connections between I/O, accelerators, and memory subsystems resulting in high-performance processors within embedded power envelopes. We take advantage of hardware accelerators to offload work on cores, which allows us to accomplish work with fewer transistors, translating to lower power. Examples of those hardware accelerators are security engines and pattern-matching engines. As we move from the P4080 device to the QorIQ AMP T4240, we are delivering more performance per watt than previously realized. Benchmarks are demonstrating a 4x performance – pretty exciting stuff.

> Where do the higher speeds come from?

BECK: The industry always speaks about improved speed, but it's really about improved performance. But first, let's address the speed. As has been done for more than 20 years, we get improved frequency with improved process geometries. We had improvement in frequency as we went from 1.5 GHz up to 2 GHz as we moved from 45 to 28 nanometer technologies while maintaining the same pipeline architecture. Additional performance improvement resulted from increasing the number of cores from 8 to 24 virtual cores. And we provide significant floating point performance with use of the AltiVec unit where the T4240 is capable of generating 192 GFLOPS.

> Let's move on to the security you mentioned earlier – where does that fit into the AMP Series of QorIQ?

BECK: I use an acronym that is applicable to the A&D market. The addition of a capital "A" to "SWaP," which makes it "SWAaP." It's about adding "Assured computing" to the long-held requirements related to Size, Weight, and Power. And it has become another critical component to every system. Every A&D RFQ or RFI has a secure or assured component. The delivery of that component cannot jeopardize the performance requirement of the mission. All future systems must be capable of withstanding security attacks. Those attacks come in the form of:

1) **Theft of functionality:** When someone is able to take over that system and cause it to act in ways that it wasn't intended to behave.
2) **Theft of uniqueness:** OEMs spend millions of dollars and years of development of systems. To see those investments efforts be reverse engineered can be disastrous.
3) **Theft of Data:** Loss of one's IP or data that is stored on the device to unauthorized parties.

> How are these challenges mitigated in the AMP Series?

BECK: We created our trust architecture capability in the P series product and have extended it in the AMP series. The primary features are secure boot, domain separation, tamper detection, and secure debug. In terms of a secure boot, you want to know that your bootable image is trusted and has not been tampered with. So, we provide the user the ability to put a secure key fused into the device. The boot process begins within the walls of your factory. With a private key, you create a 256-bit hash signature of your known trusted image. During the secure boot process, you create a signature with the key you have stored on the processor and validate that signature to the image while booting the processor. If validated, the processor is brought up in a trusted state.

Once in a trusted state, you can then begin the process of creating domain separation of cores, memory, and I/O devices. In other words, you want to distinctly define a particular relationship between cores, memory, and I/O devices in a defined partition. Domains are now able to operate independently without fear of corruption. We have intentionally designed the capability into the processor to ensure that domains are separated in the way the user wants them. This allows customers to provide separation between public, confidential, and secret regions.

Trust architecture also has the ability to react to physical threats to the system. The types of attacks are defined by the OEM.

> "All future systems must be capable of withstanding security attacks."

Some may be as simple as opening up a cabinet door. When this happens, a signal is sent to the processor and it immediately begins to zeroize the memory regions of the device. The device is now unusable and can only be made whole again through the secure boot process.

> What about network attacks?

BECK: The way we prevent network attacks is decided by the user's security policies during the secure boot process though the partitioning of the cores, memory, and I/O. Each partition is identified with a unique logical address. Network attacks come in the form of when someone will attempt to insert harmful instruction code in a particular memory region to gain control of a device's functionality. Network packets must begin authorization through a secure tunnel to the partition. Unauthorized requests are prevented from accessing a partition. A security monitor notes these attacks and notifies the OEM.

In addition, one must be able to have access to the system once it is deployed in the field. One is able to securely debug a processor, provide software upgrades, and change security policies while the system is in the field. This is done through a debug port that is entered via a question/answer handshake that the OEM has created and stored in the processor.

In the past, these types of security features [secure boot, threat detection, secure debug, and domain separation] have been external to the processor by FPGAs, TPMs [Trusted Platform Modules], or even custom devices. We have put these features inside the QorIQ processors. It has the benefit of increasing security by fewer devices and exposed buses. In addition, it decreases the overall system cost.

> Is the trust architecture user-friendly, or is it complex to navigate?

BECK: We believe we have made the implementation of the trust features user friendly. But implementation of the trust architecture is a big commitment for the user. If you ever lose your private key, it makes those systems unusable. It is a user-defined option. If you choose not to put it in trust mode, then you can use it as any processor is used today.

> One last question: What is needed now in your arena, but not available now?

BECK: It is interesting to me that there was a real fear about how quickly multicore processing would get adopted. While there is considerable need for improved software tools, the adoption has been extraordinary. The ever-increasing demand for performance within stringent power envelopes has resulted in a broad spectrum of applications. It is clearly the path we are all taking. We have just begun to deal with the challenge of certifying multicore systems in commercial aviation. While challenging, it will happen.

In addition, the fundamental challenges of system design remain: latency, bandwidth, and power. I know here at Freescale, we are constantly working to solve these real-world problems. Frankly, it's lots of fun. **MES**

Glenn Beck is Market Segment Manager for the Network Products Division, Freescale Aerospace and Defense/Single Board Computing Market. He is a 32-year semiconductor veteran with Motorola/Freescale. His experience has been in design and product engineering, and he presently leads Freescale's marketing efforts in A&D and single board computing with Power Architecture microprocessors. He holds a BS in Electrical Engineering from Texas A&M University and an MBA from Texas State University. He leads the Multicore for Avionics (MCFA) working group of avionics suppliers in an effort to certify platforms with multicore processors. He can be contacted at glenn.beck@freescale.com.

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New rugged router takes advantage of JUNOS

Focused on security, the new RTR8GE rugged router from GE Intelligent Platforms in Charlottesville, Va., is designed for thwarting cyber attacks even in heavy network traffic environments via its firewall and intrusion detection system. The COTS device uses the JUNOS operating system from Juniper Networks and provides IPv4/IPv6 connections for defense aircraft, ground vehicles, and forward operating bases that support network-centric operations.

The radio router protocols also enable radio hop efficiency and available bandwidth to be monitored in real-time to make sure quality of service is maintained, minimizing line-of-sight communications issues caused by adverse weather or other environmentally related interference.

Other security features include denial of service, IPsec, VPN, user authentication and access control, quality of service, and network address translation. The device utilizes MIL-D38999 Series 3 connectors for Ethernet ports, power, and serial connection – all in a rugged package designed for operation in -40 °C to +75 °C.

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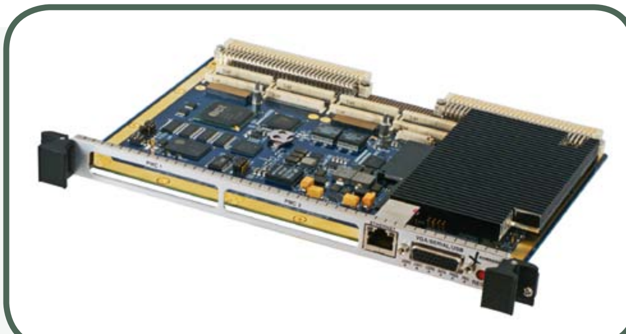
VME board compatible with any legacy system



Engineers at Xembedded, LLC are looking to improve their share of the military upgrade market with a new VME single-board computer that is compatible with any legacy system, company officials say. The COTS device can be configured to work in any VME chassis from the 2eSST to as far back as the venerable VME 32 chassis – which is more than two decades old. The design enables users of legacy VME systems to take advantage of the XVME-6300's Intel Core i7 processor configurations ranging from the 620UE for low-power applications to the 610E for those that require higher performance.

The Xembedded board comes in air- and conduction-cooled versions, operating in -40 °C to +85 °C for the conduction-cooled product and -25 °C to +70 °C for the air-cooled version. Other features include 8 GB of 1,333 MHz ECC solder memory as well as front I/O options of dual serial, quad USB 2.0, and VGS. Users can have all the I/O on the rear interface or place a large I/O amount on the front for systems without rear I/O.

Company engineers included four GbE ports with two in the front and two via the P0, configured to VITA 31.1. Standard on the boards are four 300 Mbps SATA ports, as well as options for USB flash, dual compact flash, and 2.5" or 1.8" onboard hard drive or SSD.

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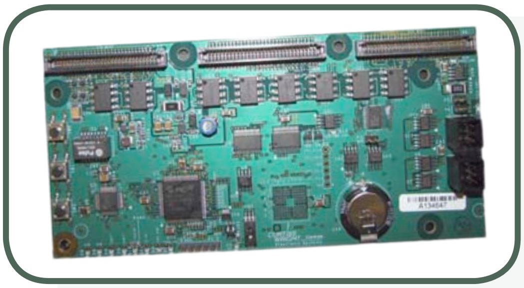
Airborne transceiver for aircraft applications

Ku-band transceivers from Wavestream – a subsidiary of Gilat Satellite Networks Ltd. – are designed to work within the size and weight requirements of manned and unmanned aircraft in military and commercial markets. The product line, which is called "AeroStream," has Ku-band transceivers in 25 W and 40 W transmit output and full Ku-band receive variants for nonpressurized and pressurized airborne applications. Company officials say the devices are well suited to meet the voice, video, and data demands of Intelligence, Surveillance, and Reconnaissance (ISR) missions of Unmanned Aerial Vehicles (UAVs). The AeroStream line meets RTCA/DO-160G, Airbus, Boeing, and ARINC requirements for commercial aircraft and MIL-STD specifications for military aircraft.

Making use of Wavestream's Spatial Power Advantage solution, the transceivers are designed to have high output power in small, lightweight, rugged packages. Both the 25 W and 40 W devices interface with many common modems and antenna control units. The company's AeroStream products can be integrated into airborne satellite communication systems based on customer-defined requirements and specifications. Ka-band support is planned for early next year.

Wavestream • www.wavestream.com • www.mil-embedded.com/p366013



Managing multiple chassis elements in one rugged module

Engineers at Curtiss-Wright Controls Electronic Systems designed the rugged Power and Control Module (PCM) single-board computer for managing chassis hardware and software elements in embedded military systems. The PCM not only provides high-level control but also bridges to system hosts through Ethernet (IEEE 802.3), USB, RS-232, and CANbus. With the ability to monitor a board's onboard software and logic, it also can be programmed to autonomously manage a computing enclosure or platform.

The PCM can also serve as a PMBus chassis management system to control Fan Controller Boards (FCBs) and intelligent power supplies. Other components of the PCM monitors are displays, front panel controls, and indicators. The new device also can direct external/internal connected devices, interactively enable/disable chassis payload power systems, and issue controlled system resets with little communication or switch interfaces. It meets MIL-STD-810G, MIL-STD-461F, and MIL-STD-704E when used in a chassis enclosure that meets these requirements.

The PCM comes in air- and conduction-cooled versions. It functions in harsh environments with an operating temperature range of -40 °C to +85 °C.

Curtiss-Wright Controls Electronic Systems • www.cwcelectronicsystems.com • www.mil-embedded.com/p366014

Streaming full-motion video from UAV to warfighter in real-time

ITT Corporation and Mercury Computer Systems engineers have joined hands to improve the speed and efficiency of how intelligence data – especially full-motion video – is disseminated to warfighters from Unmanned Aerial Vehicles (UAVs). The system – dubbed Federated Embedded inteL-server for Collaborative Operations (FELCO) – is a Processing, Exploitation, and Dissemination (PED) tool enabling warfighters to get geospatial data in real-time as opposed to hours with traditional downlink systems. The U.S. Army Project Manager-Unmanned Aircraft Systems (PM-UAS) is currently using FELCO in planned system flight tests and assessments. The FELCO system essentially compresses the PED information into real-time capture and synchronization of multiple data sources. FELCO was developed with hardware from Mercury and geospatial software from ITT. The hardware and software are scalable to enable compatibility with new sensors as they are added.

Mercury technology used in the system includes the company's Application-Ready Subsystems (ARS), which uses the Powerblock processing architecture. ITT's open-standards PED software, called "Enhanced AGILE Access," and AdLib, enable users to search/discover, serve, and store information, reducing the latency issues common for downlink systems while maintaining the integrity of the geospatial information. As small as a typical portable hard drive and also low power, FELCO can be used not only in UAV applications, but also in catapult- and runway- launched vehicles, aerostats, and civil and military fixed-mount installations.

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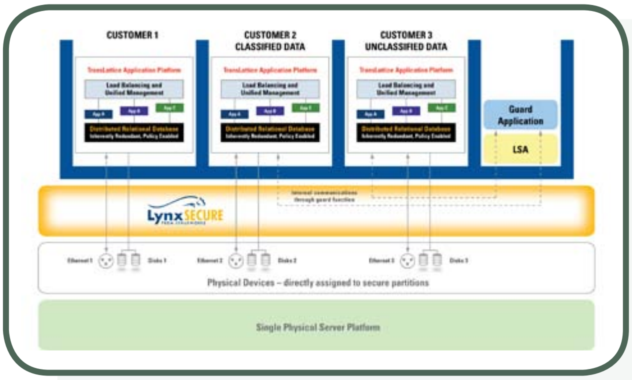

Secure cloud-based data solution created by LynuxWorks, TransLattice

Data loss in a cloud from a malware attack can be catastrophic, as the cloud is a single point of failure: If a cloud is broken into, everyone's sensitive information is at risk. Experts at LynuxWorks, Inc. and TransLattice Inc. have partnered their respective tools to minimize the impact of these attacks. They have combined virtualization techniques with distributed computing platforms to make cloud computing more secure. The TransLattice Application Platform 2.0 was ported onto the latest version of the LynxSecure separation kernel and hypervisor. Essentially LynuxWorks takes the concept of partitioning, which isolates individual applications into separate partitions so they are protected if another application is hit by a form of malware. The attacks are limited to a single partition. Communication between each partition is controlled by policies set by the system administrator and secured via another LynuxWorks tool called "LynxSecure," which enables multiple guest operating systems and their applications to run securely on a single platform.

The TransLattice Application Platform integrates physical appliances and cloud instances to create a network of distributed computing resources for running enterprise applications. Within the new solution, versions of the TransLattice platform reside in the LynxSecure partitions on a single hardware platform. This can be implemented for different classification levels for applications and data, or for multiple departments or entities that share a single cloud infrastructure.

LynuxWorks • www.lynuxworks.com • www.mil-embedded.com/p366017

TransLattice • www.translattice.com • www.mil-embedded.com/p366018

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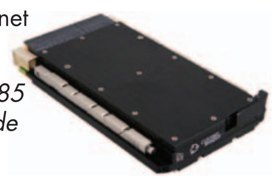

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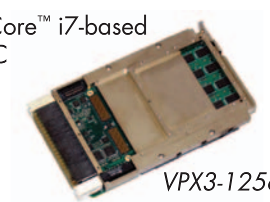

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